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Charge Coupled Semiconductor Devices

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In this paper we describe a new semiconductor device concept. Basically, it consists of storing charge in potential wells created at the surface of a semiconductor and moving the charge (representing information) over the surface by moving the potential minima. We discuss schemes for creating, transferring, and detecting the presence or absence of the charge.

In particular, we consider minority carrier charge storage at the Si-SiO_2 interface of a MOS capacitor. This charge may be transferred to a closely adjacent capacitor on the same substrate by appropriate manipulation of electrode potentials. Examples of possible applications are as a shift register, as an imaging device, as a display device, and in performing logic.

A new semiconductor device concept has been devised which shows promise of having wide application. The essence of the scheme is to store minority carriers (or their absence) in a spatially defined depletion region (potential well) at the surface of a homogeneous semiconductor and to move this charge about the surface by moving the potential minimum. A variety of functions can then be performed by having a means of generating or injecting charge into the potential well, transferring this charge over the surface of a semiconductor, and detecting the magnitude of the charge at some location. One method of producing and moving the potential wells is to form an array of conductor-insulator-semiconductor capacitors and to create and move the potential minima by applying appropriate voltages to the conductors. The purpose of this paper is to describe the operation of this basic structure and some possible applications. We present calculations which show feasibility for a simple silicon-silicon dioxide MOS structure.

First consider a single MIS structure on an n-type semiconductor. A diagram of energy vs. distance is shown in Fig. 1 for an applied voltage difference V_1 in which the metal is negative with respect to the semiconductor and large enough to cause depletion. When the

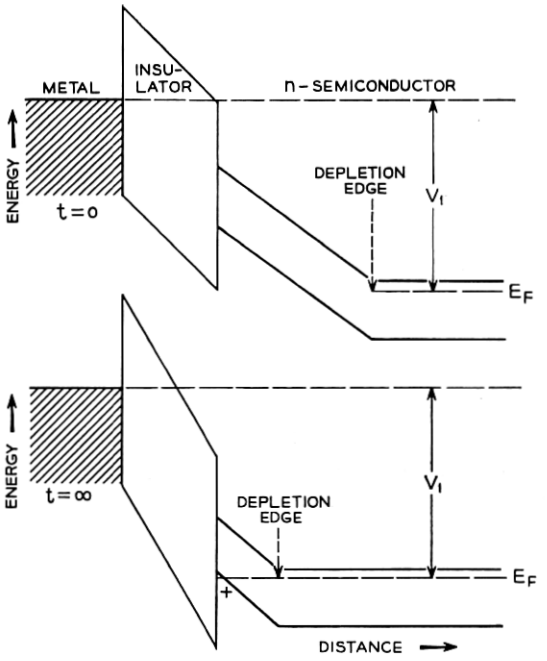

Fig. 1—A plot of electron energy vs distance through an MIS structure both with (at time $t = \infty$) and without (at time $t = 0$) charge stored at the surface.

voltage is first applied at $t = 0$, there are no holes at the semiconductor-insulator interface and the voltage is divided between the semiconductor and insulator as shown. If holes are introduced into the depletion region by some means, they will collect at the semiconductor interface causing the interface potential to become more positive. Eventually the situation shown in Fig. 1 for $t = \infty$ is reached. This is the steady state condition for the structure and it occurs when the valance band at the interface is approximately at the same energy as the Fermi level E_F in the bulk. Any further introduction of holes will cause the interface potential to become yet more positive and holes will be injected into the bulk until the steady state condition is again reached.

Now, consider the linear array of MIS structures on an n-type semiconductor as shown in Fig. 2 where every third electrode is connected to a common conductor. As an initial condition, a voltage $-V_2$ is applied to electrodes 1, 4, 7, and so on, and a voltage $-V_1$ ($V_2 > V_1$) is applied to the other electrodes. The semiconductor is held at zero potential and the V_i's are taken as positive numbers. It is assumed

that $V_1 > V_T$ where V_T is the threshold voltage for the production of inversion under steady state conditions. The edge of the depletion region is indicated by the dashed line. Also, as an example, positive charge is placed under electrodes 1 and 7 and none under electrode 4, as indicated in Fig. 2(a). Now a voltage $-V_3$ ($V_3 > V_2$) is applied to electrodes 2, 5, 8, and so on, as shown in Fig. 2(b) and the charge will transfer from electrode 1 to the potential minimum under electrode 2, and so on. The voltages are now changed to the condition of Fig. 2(c) and, as shown, charge has been shifted one spatial position and the sequence is ready to be continued.

It has been assumed in the foregoing that the voltages were applied and manipulated in a time shorter than the storage time τ where $\tau = Q/I_d$ is the time for the thermally generated current I_d to supply the equilibrium charge density Q. The thermal current I_d results from generation-recombination centers in the depletion region and at the semiconductor-insulator interface. Storage times of the order of seconds have been reported.[1-3]

It is of interest now to consider the capacitance and surface potential

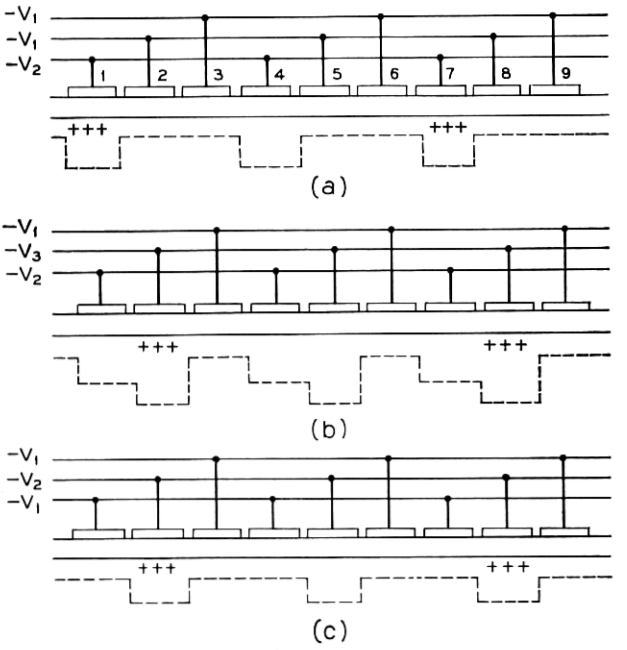

Fig. 2—Schematic of a three phase MIS charge coupled device.

of the structure as a function of stored charge. The capacitance can be used as a measure of the stored charge. Knowledge of the surface potential is necessary to design a structure that insures complete transfer of charge since, referring to Fig. 2, as charge flows from electrode 1 to electrode 2 the potential of 1 will fall and the potential of 2 will rise. Clearly the voltages V_3 and V_2 must be chosen such that the surface potential at electrode 2 is always lower. The steady state minority carrier density Q per unit area for a given gate voltage V_G is given by $Q = C_0(V_G - V_T)$ where $C_0 = K_0\epsilon_0/X_0$ is the oxide capacitance, K_0 is the oxide dielectric constant, and X_0 the thickness. For a charge density $Q' \leqq Q$, the potential φ_s at the semiconductor surface can be shown to be

$$\varphi_s = (V_G - V_{FB}) - \frac{Q'}{Q}(V_G - V_T) - \frac{B}{C_0}\left(\left\{1 + \frac{2C_0(V_G - V_{FB})}{B}\left[1 - \frac{Q'}{Q}\left(\frac{V_G - V_T}{V_G - V_{FB}}\right)\right]\right\}^{\frac{1}{2}} - 1\right) \tag{1}$$

where $B = K_s q N_D X_0/K_0$, K_s is the silicon dielectric constant, V_{FB} is the flatband voltage and N_D the donor density. Similarly, the capacitance between gate and substrate can be shown to be

$$C = C_0\left\{1 + \frac{2C_0 V_G}{B}\left[1 - \frac{Q'}{Q}\left(\frac{V_G - V_T}{V_G - V_{FB}}\right)\right]\right\}^{-\frac{1}{2}}. \tag{2}$$

These quantities are plotted as a function of Q'/Q in Fig. 3 for a representative structure with $V_T = 1.2V$. The depletion width $X_d = (2K_s\varphi_s\epsilon_0/qN_D)^{\frac{1}{2}}$ is also plotted. It is seen that these quantities are a reasonably strong function of Q'/Q for the parameters chosen. In a practical situation, the gate voltages chosen ($\sim 10V$) are readily attainable from silicon integrated circuits.

There are two interrelated quantities of interest in describing the transfer of charge from one electrode to the next. One is the time to transfer the charge and the other is the transfer efficiency which we define as the fraction of charge transferred from one electrode to the next. The time constant for transfer of charge from one electrode to another by diffusion will be of the order $\tau_0 = L^2/4D$ where L is the linear dimension of the electrode and D the diffusion constant. It is assumed that the spacings and the applied voltages are such that no potential barrier exists between the electrodes. For $L = 10^{-3}$ cm and $D = 10$ cm^2/sec, it is found that $\tau_0 = 2.5 \times 10^{-8}$ sec. The amount

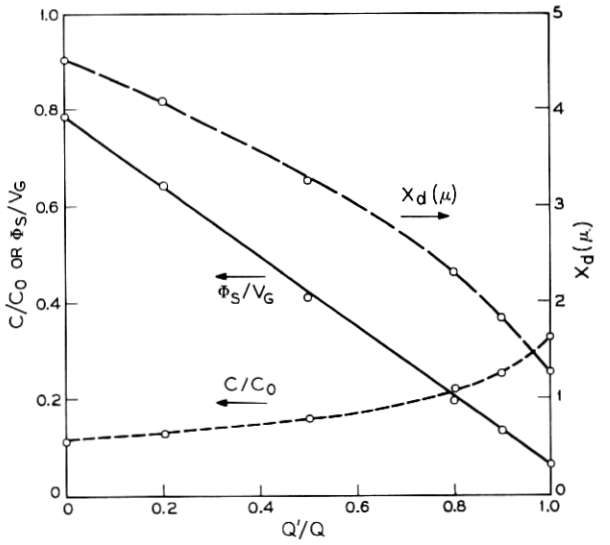

Fig. 3—A theoretical plot of depletion width (X_d), surface potential (φ_s) and capacitance (C) of an MIS structure as a function of charge at the interface (Q'). Edge effects are neglected. The values used in this calculation were:

$$V_G = 10v;$$
$$X_0 = 2 \times 10^{-5}\text{cm};$$
$$N_D = 5 \times 10^{14}/\text{cm}^3;$$
$$C_0 = 1.7 \times 10^{-8}F/\text{cm}^2.$$

of charge remaining will decay in an almost exponential manner with this time constant if trapping in deep surface and bulk states is neglected. If trapping times are comparable to any transfer times of interest, such effects will also detract from the transfer efficiency and for the current Si-SiO_2 technology, it appears that surface states will be the limiting factor.

There will also be a field enhanced component resulting from the change of surface potential with charge density. A qualitative understanding of this is obtained by considering the situation in Fig. 2(b) immediately after $-V_3$ has been applied but before charge has transferred from electrode 1 to electrode 2. As charge from the right hand edge of electrode 1 flows into the potential well under electrode 2, the potential at that edge will become more negative by an amount given by equation (1). This effect results in a field parallel to the interface which adds to the diffusion component. This field will propagate back under the electrode and decrease in magnitude as charge flows but will always add to the diffusion component. The exact nature of

this field has not been calculated but its effect is expected to be significant. For example, an average potential drop of 0.1 volts across the width of a 10^{-3} cm electrode will result in a transit time of 2.5×10^{-8} sec. assuming a mobility of 400 cm^2/v-sec. Further field enhancement may be obtained by making the electrode width plus interelectrode spacing comparable to the oxide thickness and using the fringing field of the neighboring electrode.

The structure in Fig. 2 may be used as a shift register with the addition of a charge generator at one end (input) and a detector at the other. The generation can be accomplished by a forward biased p-n junction, by surface avalanching in an MOS structure,[4] or by radiation induced pair creation. Detection may be accomplished by current detection with a reverse biased p-n junction or Schottky barrier or by utilizing the change of capacitance with charge [see equation (2)].

An estimate of the basic signal-to-noise limitations can be made by considering detection by a reversed biased diode put in place of the last electrode and connected to ground by a resistor. If Q is the average amount of charge stored in an element and f the transfer frequency, then the average signal current is simply $I_s = Qf$. For the example given in Fig. 2, $Q \approx 10^{-13}$ C for an electrode with an area of 10^{-6} cm^2. This results in a signal of 10^{-7} amperes at one megacycle. State of the art video amplifiers have an equivalent noise of about 10^{-9} amperes at one megacycle and would dominate the shot noise which for this example is 2×10^{-10} amperes.

The basic shift register concept may be used to construct a recirculating memory or used as a delay line for times up to the storage time. Clearly, charge transfer in two dimensions is possible as well as the ability to perform logic. An imaging device may be made by having a light image incident on the substrate side of the device creating electron-hole pairs. The holes will diffuse to the electrode side where they can be stored in the potential wells created by the electrodes. After an appropriate integration time, the information may be read out via shift register action. A display device[5] may be constructed by the inverse process of reading in the information (minority carriers) via shift register action and then forward biasing the MIS structure to force the minority carriers into the bulk where radiation recombination takes place.

Aside from problems of yield, the limit to the usefulness device will be determined largely by the speed of transfer, the fractional amount of charge not transferred, and the thermal discharge current. Preliminary experiments[6] show that for existing silicon technology, these parameters lie within the range of usefulness.

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Experimental Verification of the Charge Coupled Device Concept

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Structures have been fabricated consisting of closely spaced MOS capacitors on an n-type silicon substrate. By forming a depletion region under one of the electrodes, minority carriers (holes) may be stored in the resulting potential well. This charge may then be transferred to an adjacent electrode by proper manipulation of electrode potentials. The assumption that this transfer will take place in reasonable times with a small fractional loss of charge is the basis of the charge coupled devices described in the preceding paper.[1] *To test this assumption, devices were fabricated and measurements made. Charge transfer efficiencies greater than 98 percent for transfer times less than 100 nsec were observed.*

The basic principles of the charge coupled device, as already described,[1] are very simple indeed, but it is not clear whether the properties of an MIS system are adequate to give viable devices. The purpose